Claims

[c1] 1. A method for fabricating a nitride read-only memory, comprising:
forming a silicon oxide/silicon nitride/silicon oxide (ONO) stacked layer on a substrate, the ONO stacked layer consisting of a bottom oxide layer, a silicon nitride layer and a top oxide layer;
forming a protective layer on the ONO stacked layer;
patterning the protective layer and the ONO stacked layer to form a plurality of stacked patterns, wherein an etching rate of the protective layer is lower than an etching rate of the top oxide layer; and
removing the protective layer.

[c2] 2. The method of claim 1, wherein removing the protective layer comprises using wet etching to remove the protective layer.

[c3] 3. The method of claim 1, wherein a thickness of the bottom oxide layer is about 50~100 Å .

[c4] 4. The method of claim 1, wherein a thickness of the silicon nitride layer is about 55~80 Å .

[c5] 5. The method of claim 1, wherein a thickness of the top oxide layer is about 70~120 Å .

[c6] 6. The method of claim 1, the protective layer comprises silicon nitride.

[c7] 7. The method of claim 1, wherein a thickness of the protective layer is smaller than 50 Å .

[c8] 8. The method of claim 1, further comprising:
performing an ion implantation to form a plurality of buried bit lines in the substrate between the stacked patterns;
forming an insulator on each buried bit line; and
forming a plurality of word lines on the substrate.

[c9] 9. The method of claim 8, wherein the ONO stacked layer is patterned until a portion of the bottom oxide layer is exposed.

[c10] 10. The method of claim 9, wherein the exposed bottom oxide layer is removed after the ion implantation is performed.

[c11] 11. The method of claim 8, wherein the insulator comprises silicon oxide.

[c12] 12. The method of claim 8, wherein the word lines comprise polysilicon.

[c13] 13. A method for fabricating a nitride read-only memory, comprising:
forming a silicon oxide/silicon nitride/silicon oxide (ONO) stacked layer on a substrate, the ONO stacked layer consisting of a bottom oxide layer, a silicon nitride layer and a top oxide layer;
forming a protective layer on the ONO stacked layer, the protective layer having a thickness smaller than 50 Å ;
patterning the protective layer and the ONO stacked layer to form a plurality of stacked patterns, wherein an etching rate of the protective layer is lower than an etching rate of the top oxide layer;
performing an ion implantation to form a plurality of buried bit lines in the substrate between the stacked patterns;
forming an insulator on each buried bit line; and
forming a plurality of word lines on the substrate.

[c14] 14. The method of claim 13, wherein a thickness of the bottom oxide layer is about 50~100 Å .

[c15] 15. The method of claim 13, wherein a thickness of the silicon nitride layer is about 55~80 Å .

[c16] 16. The method of claim 13, wherein a thickness of the top oxide layer is about 70~120 Å .

[c17] 17. The method of claim 13, the protective layer comprises silicon nitride.

[c18] 18. The method of claim 13, the insulator comprises silicon oxide.

[c19] 19. The method of claim 13, wherein the word lines comprise polysilicon.

[c20] 20. The method of claim 13, wherein the ONO stacked layer is patterned until a portion of the bottom oxide layer is exposed.

[c21] 21. The method of claim 20, wherein the exposed bottom oxide layer is removed after the ion implantation is performed.